

a pre-metal dielectric layer between said lowermost metal interconnect layer and the semiconductor substrate, the pre-metal dielectric comprising an at least substantially porous dielectric material doped with at least one dopant.

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(continued)
22. The integrated circuit of claim 21, wherein said at least one dopant comprises phosphorus.

23. The integrated circuit of claim 21, wherein said at least one dopant comprises fluorine.

24. The integrated circuit of claim 21, wherein said at least one dopant comprises carbon.

25. The integrated circuit of claim 21, wherein said at least one dopant comprises boron.